memory cell of the NVRAM device, to reset the memory cell, wherein the reset mirror voltage is lower than the selection mirror voltage, to facilitate delivery of a reset current above a current threshold to the memory cell.

[0049] Example 11 may include the subject matter of Example 10, wherein applying a selection mirror voltage includes applying voltage that is approximately equal to an inhibit voltage associated with the NVRAM device.

[0050] Example 12 may include the subject matter of Example 10, wherein applying a selection mirror voltage to an NVRAM device includes: coupling a selection mirror circuit with the NVRAM device; and providing the selection mirror voltage, with the selection mirror circuit, to the NVRAM device.

[0051] Example 13 may include the subject matter of Example 10, wherein applying a reset mirror voltage to the memory cell of the NVRAM device includes: coupling a reset mirror circuit with the NVRAM device; and providing the reset mirror voltage, with the reset mirror circuit, to the memory cell.

[0052] Example 14 may include the subject matter of Example 12, wherein coupling a selection mirror circuit with the NVRAM device includes connecting the selection mirror circuit with a word line of the NVRAM device, wherein the memory cell is coupled with the word line.

[0053] Example 15 may include the subject matter of Example 14, wherein coupling a reset mirror circuit with the NVRAM device includes connecting the reset mirror circuit with the word line of the NVRAM device.

[0054] Example 16 may include the subject matter of any of Examples 10 to 15, wherein applying a reset mirror voltage includes applying the reset mirror voltage after a snap-back event of the memory cell, wherein the snap-back event occurs in response to applying the selection mirror voltage to the NVRAM device, wherein the NVRAM device is a phase change memory (PCM) device.

[0055] Example 17 is a mobile device, comprising: a processor; and a memory coupled with the processor, wherein the memory includes: a phase change memory (PCM) device; a selection mirror circuit coupled with the PCM device to apply a selection mirror voltage to the PCM device, to select a memory cell of the PCM device; and a reset mirror circuit coupled with the PCM device to apply a reset mirror voltage to the memory cell of the PCM device, subsequent to the application of the selection mirror voltage, to reset the memory cell, wherein the reset mirror voltage is lower than the selection mirror voltage, to facilitate delivery of a reset current above a current threshold to the memory cell.

[0056] Example 18 may include the subject matter of example 17, wherein the reset mirror circuit to apply a reset mirror voltage to the memory cell of the PCM device, subsequent to the application of the selection mirror voltage, includes to apply the reset mirror voltage after a snap-back event of the memory cell, wherein the snap-back event occurs in response to the application of the selection mirror voltage to the PCM device.

[0057] Example 19 may include the subject matter of Example 18, wherein the memory cell is coupled with a word line of the PCM memory device, and wherein the selection mirror circuit and reset mirror circuit are connectable with the word line, to apply the selection mirror voltage and reset mirror voltage to the memory cell.

[0058] Example 20 may include the subject matter of Example 19, wherein the snap event occurs when a voltage across the memory cell exceeds a threshold voltage, in response to the application of the selection mirror voltage to the word line.

[0059] Example 21 may include the subject matter of any of Examples 17 to 19, wherein the selection mirror circuit to apply a selection mirror voltage includes to apply a voltage value that is approximately equal to an inhibit voltage associated with the PCM memory device.

[0060] Computer-readable media (including non-transitory computer-readable media), methods, apparatuses, systems, and devices for performing the above-described techniques are illustrative examples of embodiments disclosed herein. Additionally, other devices in the above-described interactions may be configured to perform various disclosed techniques.

[0061] Although certain embodiments have been illustrated and described herein for purposes of description, a wide variety of alternate and/or equivalent embodiments or implementations calculated to achieve the same purposes may be substituted for the embodiments shown and described without departing from the scope of the present disclosure. This application is intended to cover any adaptations or variations of the embodiments discussed herein. Therefore, it is manifestly intended that embodiments described herein be limited only by the claims.

What is claimed is:

1. An apparatus, comprising:

a non-volatile random access memory (NVRAM) device;

a selection mirror circuit coupled with the NVRAM device to apply a selection mirror voltage to the NVRAM device, to select a memory cell of the NVRAM device; and

a reset mirror circuit coupled with the NVRAM device to apply a reset mirror voltage to the memory cell of the NVRAM device, subsequent to the application of the selection mirror voltage, to reset the memory cell,

wherein the reset mirror voltage is lower than the selection mirror voltage, to facilitate delivery of a reset current above a current threshold to the memory cell.

2. The apparatus of claim **1**, wherein the selection mirror circuit to apply a selection mirror voltage includes to apply a voltage value that is approximately equal to an inhibit voltage associated with the NVRAM device.

3. The apparatus of claim **1**, wherein the NVRAM device is a PCM device, and wherein the memory cell includes a phase change material coupled with an ovonic threshold switch (OTS), and wherein the reset mirror voltage, applied to the memory cell, is to convert the phase change material from a crystalline state to an amorphous state.

4. The apparatus of claim **1**, wherein the select mirror voltage is about −3.5 V, wherein the reset mirror voltage is about −4.25 V.

5. The apparatus of claim **1**, wherein the reset mirror circuit to apply a reset mirror voltage to the memory cell of the NVRAM device, subsequent to the application of the selection mirror voltage, includes to apply the reset mirror voltage after a snap-back event of the memory cell, wherein the snap-back event occurs in response to the application of the selection mirror voltage to the NVRAM device.

6. The apparatus of claim **5**, wherein the memory cell is coupled with a word line of the NVRAM device, and wherein the selection mirror circuit and reset mirror circuit